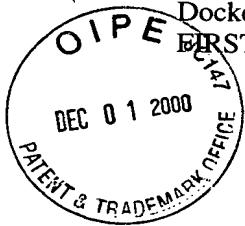


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Docket No.: 1000-052
FIRST CLASS MAIL

UTILITY PATENT APPLICATION

#2 | CFR
8.2-01
A. States

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kai Yang
 Serial No.: 09/663,021 : Group Art Unit: 2811
 Filed: 09/15/2000 : Data Entry: Rorie, Deanna
 For: SELF-ALIGNED SEMICONDUCTOR INTERCONNECT BARRIER
 AND MANUFACTURING METHOD THEREFOR

Assistant Commissioner for Patents
 Office of Initial Patent Examination
 Customer Service
 Washington, D.C. 20231

TRANSMITTAL and REQUEST TO CORRECT FILING RECEIPT

Sir:

With regard to the Filing Receipt dated 11/13/2000, in the Applicant(s) section there is an error with respect to the following:

INCORRECT:

Kai Young, San Jose, CA

CORRECT:

Kai Yang, San Jose, CA

Takeshi Nogami, Kanagawa, Japan

Dirk Brown, Sunnyvale, CA

Shekhar Pramanick, Fremont, CA

Please correct the error, and provide a corrected Filing Receipt. A copy of the Declaration is included. No additional fee is required. The correction is not due to any error by applicant and no fee is due. At any time during the pendency of this application, please charge any fees required for credit any overpayment to Deposit Account 01-0365 pursuant to 37 CFR 1.25.

The following documents are enclosed:

- Executed Declarations and Power of Attorney.

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Copy of Filing Receipt dated 11/13/00.

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Respectfully submitted,



Mikio Ishimaru
Attorney for Applicant(s)
Registration No. 27,449

The Law Offices of Mikio Ishimaru
1046 Pinenut Court
Sunnyvale, CA 94087
Telephone: (408) 738-0592
November 28, 2000

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/663,021	09/15/2000	2811	690	D412	2	18	3

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Applicant(s)

FIX

TO ↓

Kai Young, San Jose, CA; YANG

① ADD - Takeshi Nogami, Kanagawa, Japan,
Continuing Data as Claimed by Applicant

THIS APPLN CLAIMS BENEFIT OF 60/154,606 09/17/1999

Foreign Applications

② ADD - Dirk Brown, Sunnyvale, CA

③ ADD - Shekhar Pramanick, Fremont, CA

If Required, Foreign Filing License Granted 11/09/2000

Title

Self-aligned semiconductor interconnect barrier and manufacturing method therefor

Preliminary Class

257

Data entry by : RORIE, DEANNA

Team : OIPE

Date: 11/13/2000



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